Synthesis Flow of xpipes Components

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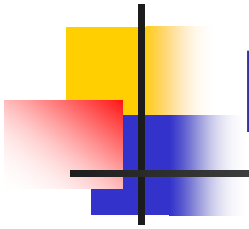
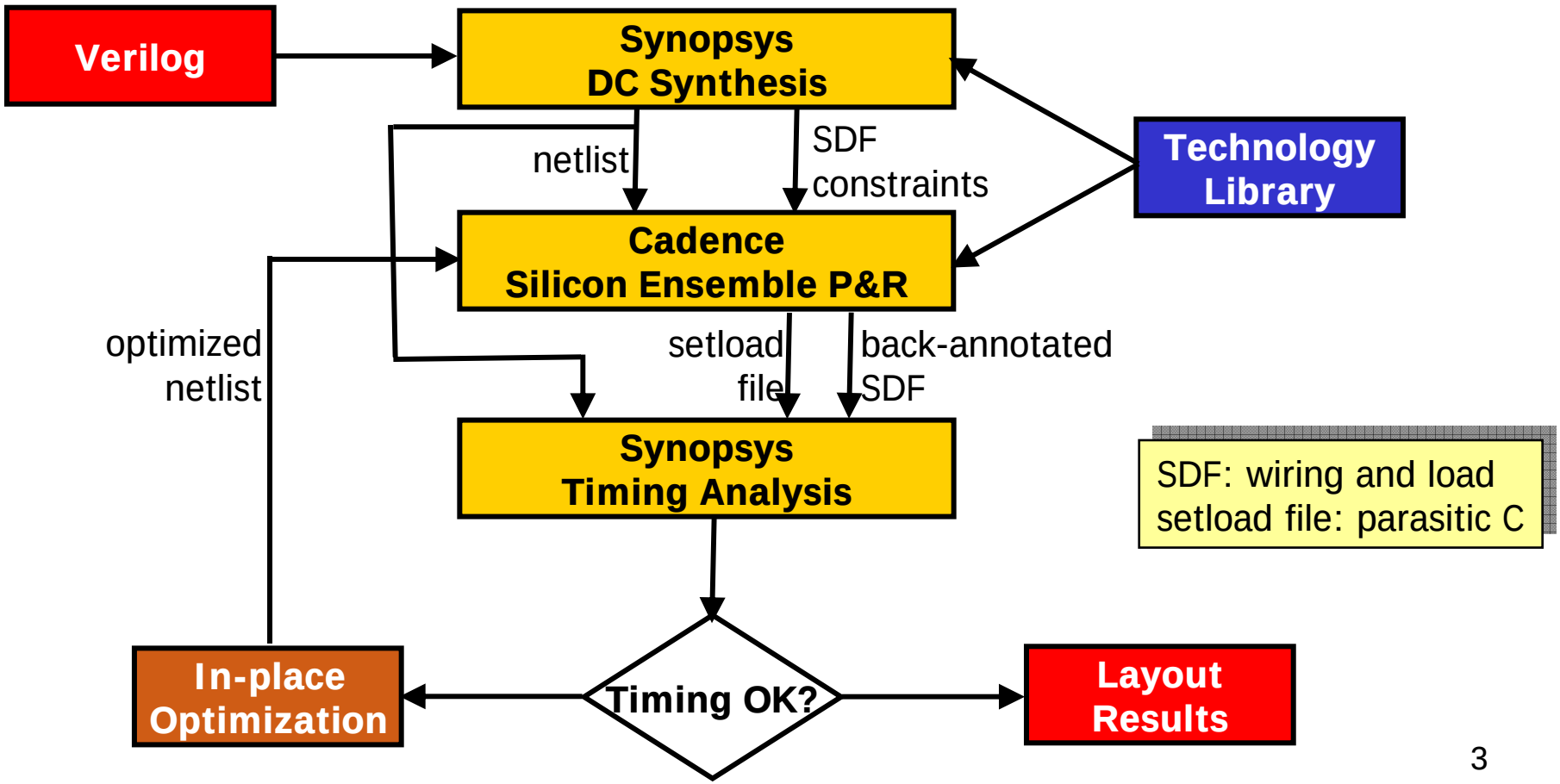
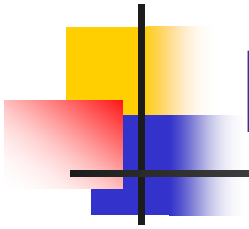


Establishing a Synthesis Flow

- Aims:
  - Pre- and post-layout verification
  - Clock frequency assessment
  - Area utilization
  - Power characterization
- Currently only fully available on UMC 0.13 µm due to layout info required in the technology library (and unavailable for ST)

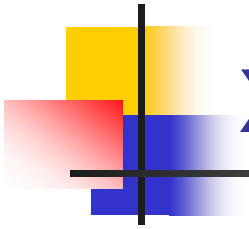
Layout Generation Flow





Layout Constraints

- Row utilization was set to 85% (margin for clock & power nets)
- Before final tapeout, when chip is complete, new in-place optimization might be run to trim away any empty area
- Slack violations resulting from P&R can be fixed in-place



xpipes Validation

- On a simple testbench topology with traffic generators:
  - ✓Pre-synthesis SystemC
  - ✓Pre-synthesis Verilog
  - ✓Post-synthesis netlist
  - ✓Layout

Clock and Area Assessment

- Max frequency results, on UMC library, for 16-bit switches with 6 output buffer stages:

	Netlist		**Layout** **(85% utilization)**	
	Area (mm^2)	Frequency (MHz)	Area (mm^2)	Frequency (MHz)
4x4 switch	0.050	667	0.059	667
12x12 switch	0.250	495	0.294	495

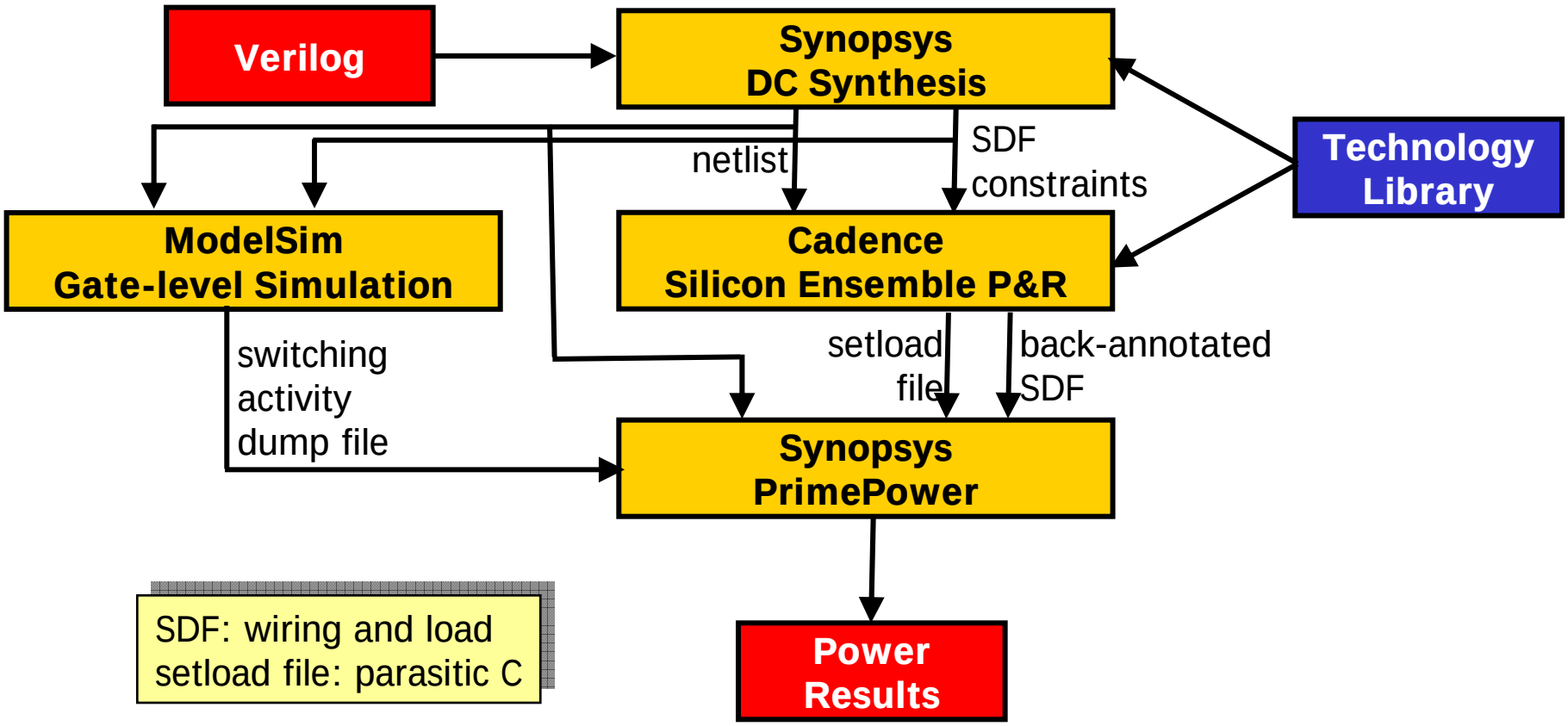
- Results not comparable to DATE05 (ST library); less area, but 30% less MHz

DATE05 Switch Area Results

Area (mm^2)

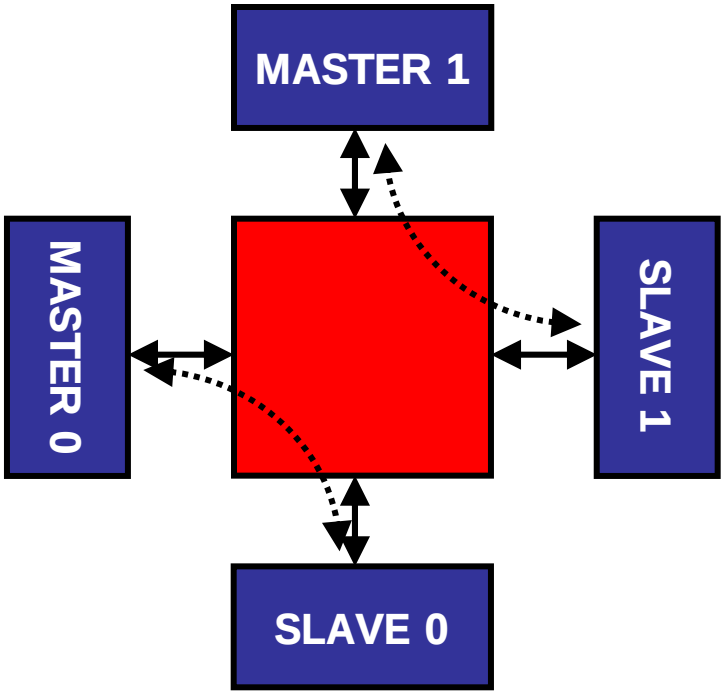
Flit Width	Output Buffer Stages 4	16
4x4 Switches		
16	0.054 @ 1 GHz	0.126 @ 1 GHz
32	0.091 @ 1 GHz	0.214 @ 1 GHz
64	0.161 @ 1 GHz	0.378 @ 1 GHz
128	0.311 @ 1 GHz	0.777 @ 1 GHz
4x6 Switches		
16	0.091 @ 990 MHz	0.226 @ 950 MHz
32	0.151 @ 970 MHz	0.389 @ 950 MHz
64	0.287 @ 970 MHz	0.777 @ 915 MHz
128	0.518 @ 925 MHz	1.637 @ 900 MHz
6x4 Switches		
16	0.070 @ 980 MHz	0.167 @ 900 MHz
32	0.112 @ 950 MHz	0.268 @ 900 MHz
64	0.213 @ 935 MHz	0.533 @ 890 MHz
128	0.400 @ 875 MHz	1.028 @ 830 MHz

Power Modeling Flow



Power Characterization Testbench

- Power dissipation was modeled on testbench with continuous traffic stream



Power Assessment

4x4 switch	Dynamic	Leakage	Total
Average	19.38 mW	0.03 mW	19.41 mW
Average %	99.998%	0.002%	100%
Peak	53.75 mW	0.03 mW	53.78 mW

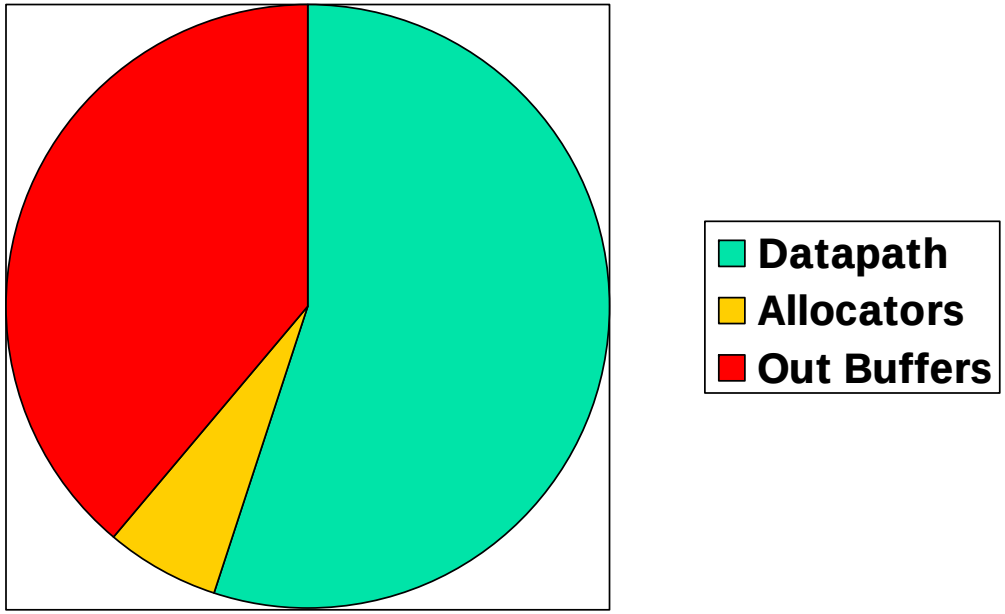
- Not comparable to DATE05 at all
- But luckily way lower than that

DATE05 Switch Power Results

Power (*mW*)

Flit Width	Output Buffer Stages 4	16
4x4 Switches		
16	31.1	62.7
32	[illegible]	116.9
64	104.4	219.3
128	199.1	430.5
4x6 Switches		
16	42.8	90.1
32	79.7	170.8
64	148.2	334.4
128	283.2	617.3
6x4 Switches		
16	35.9	69.1
32	62.9	123.2
64	117.2	237.6
128	223.4	453.5

Power Breakdown



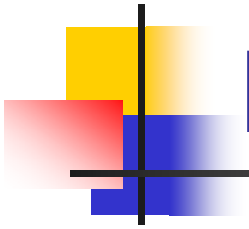
- Dominant contibution: datapath (input latch + crossbar) and output buffers

Proposed Power Model

- Tests with incoming traffic and when idle
- Model might be:

P = f(traffic, config)
where
config = {flitwidth, #inputs, #outputs, #buffers}

- Hopefully flow control and arbitration policies should not matter much



Future Work

- Network Interface power models?...
- Lots of additional exploration & optimizations
- Full-custom synthesis of critical blocks
  - crossbar
  - buffers (dual-ported memories)